1. An integrated circuit comprising:

a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time.

2. The integrated circuit of claim 1 further comprising:

a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer; and

a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer.

3. The integrated circuit of claim 1 further comprising:

a first retimer for retiming said first time-division multiplexed signal; and

a second retimer for retiming said second time-division multiplexed signal.

4. The integrated circuit of claim 1 further comprising:

an output port; and

a cross-connect for outputting at least a portion of said first time-division multiplexed signal via said output port.

5. A method comprising:

receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

indicating, at a point in time, how far said first time-division multiplexed signal is from a frame boundary; and

indicating, at said point in time, how far said second time-division multiplexed signal is from a frame boundary.

6. The method of claim 5 further comprising:

storing said first time-division multiplexed signal into a first memory at a location that is indicated by a first write pointer;

reading said first time-division multiplexed signal from a location in said first memory that is indicated by a first read pointer;

storing said second time-division multiplexed signal into a second memory at a location that is indicated by a second write pointer; and

reading said second time-division multiplexed signal from a location in said second memory that is indicated by a second read pointer.

7. The method of claim 5 further comprising:

retiming said first time-division multiplexed signal in accordance with a clock signal; and

retiming said second time-division multiplexed signal in accordance with said clock signal.

8. An apparatus comprising:

a first integrated circuit comprising:

(i) a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

(ii) a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries;

(iii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

(iv) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and

a second integrated circuit comprising a controller for reading the contents of said first frame position register and said second frame position register.

9. The apparatus of claim 8:

wherein said first integrated circuit further comprises:

(v) a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer; and

(vi) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer; and

wherein said controller is further for storing a value in said first write pointer based on the contents of said first frame position register and said second frame position register.

10. The apparatus of claim 9 wherein said first integrated circuit further comprises:

(vii) an output port; and

(viii) a cross-connect for outputting at least a portion of said first time-division multiplexed signal via said output port.

11. A composite switch comprising:

a first integrated circuit comprising:

(i) a first input port for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries;

(ii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and

a second integrated circuit comprising:

(i) a second input port for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries, and

(ii) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and

a controller for reading the contents of said first frame position register and said second frame position register.

12. The composite switch of claim 11 further comprising a third integrated circuit for outputting said first time-division multiplexed signal to said first integrated circuit and for outputting said second time-division multiplexed signal to said second integrated circuit.

13. The composite switch of claim 12:

wherein said first integrated circuit further comprises:

(iii) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer; and

wherein said first integrated circuit further comprises:

(iii) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer.

15. The composite switch of claim 14 wherein said controller is further for storing a value in said first write pointer based on the contents of said first frame position register and said second frame position register.

16. A composite switch comprising:

a first integrated circuit for outputting a first time-division multiplexed signal that comprises a first series of frame boundaries to a second integrated circuit and for outputting a second time-division multiplexed signal that comprises a second series of frame boundaries to a third integrated circuit;

wherein said second integrated circuit comprises:

(i) a first input port for receiving said first time-division multiplexed signal,

(ii) a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer,

(iii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a first point in time, and

(iv) a first output port for outputting a third time-division multiplexed signal that is based on said first time-division multiplexed signal and that comprises a third series of frame boundaries;

wherein said third integrated circuit comprises:

(i) a second input port for receiving said second time-division multiplexed signal,

(ii) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer,

(iii) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said first point in time, and

(iv) a second output port for outputting a fourth time-division multiplexed signal that is based on said second time-division multiplexed signal and that comprises a fourth series of frame boundaries;

a fourth integrated circuit comprising:

(i) a third input port for receiving said third time-division multiplexed signal,

(ii) a third memory that stores said third time-division multiplexed signal at a location that is indicated by a third write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a third read pointer,

(iii) a third frame position register whose contents are related to how far said third time-division multiplexed signal is from a frame boundary in said third time-division multiplexed signal at a second point in time,

(iv) a fourth input port for receiving said fourth time-division multiplexed signal,

(v) a fourth memory that stores said fourth time-division multiplexed signal at a location that is indicated by a fourth write pointer and that reads said fourth time-division multiplexed signal at a location that is indicated by a fourth read pointer,

(vi) a fourth frame position register whose contents are related to how far said fourth time-division multiplexed signal is from a frame boundary in said fourth time-division multiplexed signal at said second point in time; and

a controller for reading the contents of said first frame position register and said second frame position register, for storing a value in said first write pointer based on the contents of said first frame position register and said second frame position register, for reading the contents of said third frame position register and said fourth frame position register, and for storing a value in said third write pointer based on the contents of said third frame position register and said fourth frame position register.

17. The composite switch of claim 16 wherein said first point in time and said second point in time are the same.